US – 405

IV Semester B.Sc. Examination, May 2017
(CBCS) (2015-16 and Onwards) (Fresh+Repeaters)
ELECTRONICS – IV
Digital Electronics and Verilog

Time : 3 Hours Max. Marks : 70

Instructions: *Answer **all** questions from Part – **A**, **any five** questions from Part – **B** and **any four** questions from Part – **C**.*

Note: *It is required to answer **all** the questions of Part – **A** in **any one** page and to be answered only **once**. In this Part answering the **same** question multiple times will **not** be considered for evaluation.*

PART – A

Answer **all** the subdivisions : **(15×1=15)**

1. i) The output of a gate is LOW only when all the inputs are HIGH. The gate is
   a) AND b) NAND c) OR d) NOR

   ii) The maxterm representation of $A + \bar{B} + C$ is
   a) M_2 b) M_4 c) M_5 d) M_3

   iii) In a 4 variable K-map, an octet eliminates
   a) Three variables and their complements
   b) Two variables and their complements
   c) One variable and its complement
   d) Four variables and their complements

   iv) In a certain digital waveform, the period is twice the pulse width. The duty cycle is
   a) 100% b) 66% c) 50% d) 0%

   v) The input to a BCD-to-7 segment decoder is 0101. The active outputs are
   a) a, c, f, g b) a, b, c, f, g, c) b, c, e, f d) a, c, d, f, g

   vi) The IC 74147 is
   a) Decimal to BCD priority encoder
   b) BCD to decimal decoder
   c) BCD to 7-segment decoder
   d) 4-bit magnitude comparator

P.T.O.

vii) In a negative edge triggered JK flip-flop, J=K=1. The clock frequency is 10 kHz. The frequency of Q output is

a) 20 kHz b) 10 kHz c) 5 kHz d) 1 kHz

viii) A three – bit counter has _____ possible natural counts.

a) 7 b) 8 c) 9 d) 12

ix) _____ has the highest priority in a JK flip-flop.

a) J input b) K input c) Preset input d) Clock input

x) In Verilog, the bit pattern for the constant 12' h13x is

a) 0001101xxxxx b) 00001101xxxx

c) 00010011xxxx d) 000011010000

xi) In verilog 'h1234 is a

a) 16 bit number b) 32 bit number

c) 64 bit number d) 8 bit number

xii) Which is the correct method of specifying time scale in verilog ?

a) 110ns/10ps b) 100ns/10ps c) 100ns/12ps d) 101ns/10ps

xiii) In the verilog statement *assign # (4, 8) a = b;* the turn off delay is

a) 4 time units b) 8 time units c) 4 ns d) 8 ns

xiv) The statements in a *begin ... end* block are executed

a) Concurrently b) Sequentially

c) Randomly d) None of the above

xv) initial

```
begin
   #5 x = 1'b0 ;    //statement 1
   #15y = 1'b1 ;    //statement 2
end
```

In the above verilog code, the statement 2 will be executed at

a) 15 time units b) 20 time units

c) 5 time units d) Current simulation time

PART – B

Answer **any five** questions : **(5×7=35)**

2. a) Realize AND, EXOR, OR and NAND gates using only NOR gates.

   b) Draw the circuit of a CMOS inverter and explain its operation. **(4+3)**

3. What is a decoder ? Draw the logic circuit of a 3 : 8 decoder with active LOW outputs. Explain its operation with the help of its truth table. **7**

4. a) With a neat circuit diagram explain the operation of a 4 – bit Digital-to-analog converter with binary weighted resistors. Write the expression for its analog output.

   b) Write the truth table of a full adder. **(5+2)**

5. a) Explain the operation of a negative edge triggered JK flip-flop with its block diagram. Write its truth table and timing diagram.

   b) What are preset and clear inputs in a flip-flop ? **(5+2)**

6. Design a mod – 5 synchronous counter using K – Map technique. **7**

7. a) Distinguish between *wor* and *tril* nets with their syntax and truth tables.

   b) Define the terms synthesis, test bench and vector net. **(4+3)**

8. a) Describe dataflow style of verilog. How does it differ from behavioural style ?

   b) With the help of a circuit diagram, write a verilog code for 4 : 2 encoder in dataflow style. Also write its truth table. **(4+3)**

9. Explain the procedural and continuous assignments in verilog with examples for each.

PART – C

Answer **any four** questions : **(4×5=20)**

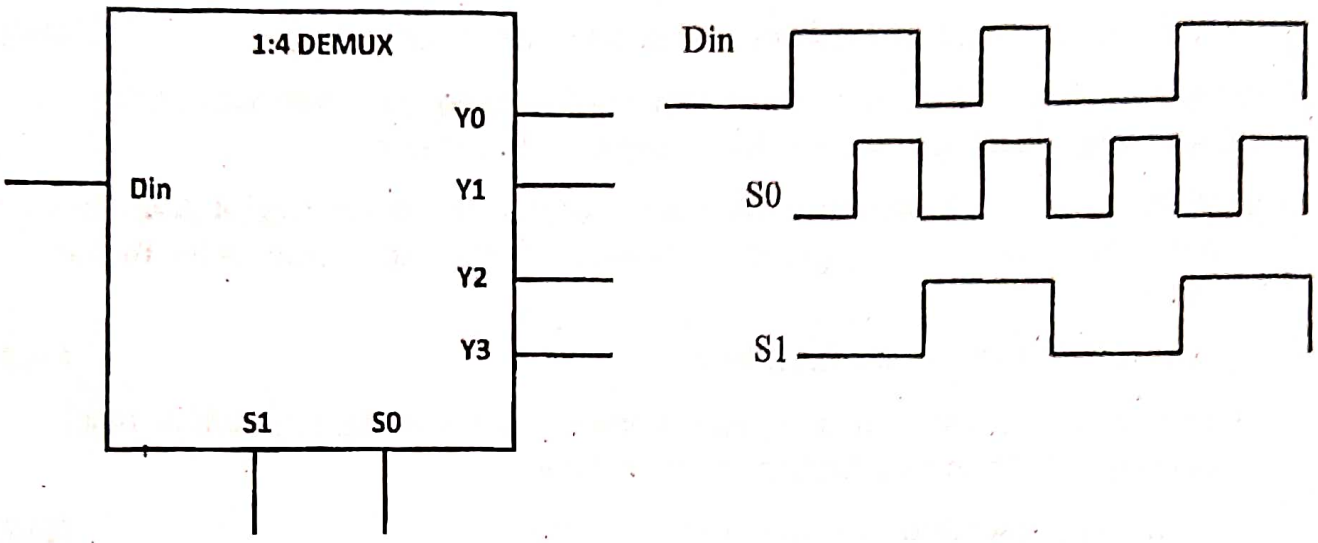
10. Simplify the following Boolean expression and implement the simplified expression.

$$Y = \overline{(\overline{AB}.C) . \overline{CD} + D}$$ **5**

11. Using K-map simplify the following Boolean expression and realize the simplified expression using gates. **5**

$Y(A, B, C, D) = \Sigma m(5, 7, 8, 10, 13, 15)$ and don't care condition
$d(A, B, C, D) = \Sigma m(0, 1, 2, 6)$.

12. Draw the output waveforms for Y0, Y1, Y2 and Y3 for the given inputs. 5



13. Draw the logic circuit diagram of a 4-bit Serial-in-serial-out shift register and explain its operation taking the data 1101 as an example. 5

14. Write a verilog code to implement full subtractor. Write its truth table. 5

15. Write a verilog code to implement 2 – bit magnitude comparator. 5