SM – 421

IV Semester B.Sc. Examination, May/June 2018
(CBCS) (Fresh+Repeaters) (2015 – 16 & Onwards)
ELECTRONICS – IV
Digital Electronics and Verilog

Time : 3 Hours

Max. Marks : 70

Instructions : *1) Answer **all** the questions from Part – A, **any five** questions from Part – **B** and **any four** questions from Part – **C**.*

*2) It is required to answer **all** the questions of Part – **A** in **any one** page and to be answered only **once**. In this Part, answering the **same** question multiple times will not be considered for evaluation.*

PART – A

Answer **all** the subdivisions. **(15×1=15)**

1. i) The term bit refers to
   a) a small amount of data b) collection of digits
   c) binary digit d) none of the above

   ii) An inverter
   a) performs the NOT operation
   b) changes a HIGH to LOW
   c) changes a LOW to HIGH
   d) all the above

   iii) In a certain digital circuit, the time period of the applied signal is twice the pulse width. The duty cycle is
   a) 100% b) 200% c) 50% d) 66.66%

   iv) A 3-variable Karnaugh Map has
   a) eight cells b) three cells
   c) sixteen cells d) four cells

   v) The device used to convert a binary number to a decimal format is
   a) multiplexer b) encoder c) decoder d) register

P.T.O.

vi) In a 4-bit binary weighted resistor type D/A converter most significant bit resistor is 10 KΩ. The least significant bit resistor used in

a) 1.25 KΩ b) 12.5 KΩ c) 40 KΩ d) 80 KΩ

vii) A flip-flop is

a) 2-bit memory b) 1-bit memory

c) not a memory d) a combinational circuit

viii) The content of a 4-bit register is 1000. The register is shifted 3 times to the right. The content of the register will be

a) 1001 b) 0011 c) 0001 d) 1000

ix) A BCD counter is an example of

a) a full modulus counter b) a decade counter

c) a modified counter d) both (b) and (c)

x) In order to build a mod-7 up counter the minimum number of flip flops required is

a) 4 b) 2 c) 1 d) 3

xi) Which of the following statements are wrong with respect to Verilog ?

a) Relatively harder to learn b) Extra white space is ignored

c) Keywords are in lowercase d) Comments may not be nested

xii) Default value of variable data type is

a) 0 b) X c) Z d) 1

xiii) In Verilog the identifier beginning with _____ character is interpreted as a system task or as system function.

a) # b) // c) $ d) ^

xiv) If A = 4`b0011 and B = 4b`0011, then the result of A**B will be

a) 6 b) 3 c) 9 d) 27

xv) Which is not a correct method of specifying time scale in verilog ?

a) 1 ns/1 ps b) 10 ns/1 ps c) 100 ns/100 ps d) 100 ns/110 ps

PART – B

Answer **any five** questions : **(5×7=35)**

2. a) Verify the universal property of NAND gate by realizing AND, OR and XOR gates.

   b) State and prove De Morgan's theorems. **(3+4)**

3. a) What is half adder ? Draw the circuit diagram using logic gates and write its truth table.

   b) What is a magnitude comparator ? Draw the logic diagram of a two bit magnitude comparator using XOR and AND gates. **(4+3)**

4. a) With a relevant circuit diagram, explain the working of 4-bit binary weighted D to A converter.

   b) Draw the logic circuit of 2 : 4 decoder using AND gates. **(5+2)**

5. a) Explain the working of D flip-flop with circuit diagram. Draw the truth table and timing diagram.

   b) Draw the truth table and timing diagram of T-flip-flop. **(5+2)**

6. What is a shift register ? Draw the logic diagram of a 4-bit serial-in parallel-out shift register. Explain how the data 0111 is written and retrieved. Also draw the timing diagram. **7**

7. a) Compare VHDL and Verilog.

   b) Write the basic module of Verilog programming. **(5+2)**

8. Explain arithmetic and logical operators in Verilog with examples. **7**

9. Explain the statements if, if-else and if – else, if --- else in Verilog. **7**

PART – C

Answer **any four** questions : **(4×5=20)**

10. Simplify the expression $A \cdot \bar{B} \cdot C + A \cdot \bar{C} + \bar{A} \cdot B\,(B \cdot C + \bar{B})$ using Boolean laws and draw the circuit for simplified expression using basic gates. **5**

11. Simplify the Boolean function $f(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + \sum d(2, 13)$ using K-map and realize the simplified expression using basic gates. **5**

12. A 4-bit digital to analog converter has a step size of 0.5 V. Determine full scale output voltage and percentage of resolution. **5**

13. Design a synchronous mod-5 counter using K-map technique. **5**

14. Write a Verilog code for all the logic gates. **5**

15. Write a Verilog code for 4 : 1 multiplexer. **5**